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INPUT/OUTPUT BUS CYCLE CONTROL CIRCUIT
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Specifications

/369[1]

1. Title of the Invention

Input/Output Bus Cycle Control Circuit

2. Claim(s)

A circuit in which an idle clock is inserted between the end of an input/output bus cycle and the start of the following input/output bus cycle of a system controlled by a microprocessor;

an input/output bus cycle control circuit characterized by being equipped with

a 1st storage means for storing the recovery time of a peripheral device,

a detecting means terminal for detecting the operating frequency of the aforesaid system,

a converting means for converting the recovery time stored in the aforesaid 1st storage means to the number of idle clocks associated with the operating frequency of the aforesaid system, and

a 2nd storage means for storing the number of idle clocks found by the aforesaid converting means; and

always inserting the correct idle clock within the input/output bus cycle even if the operating frequency of the system changes.

3. Detailed Specifications

Field of Industrial Application

The present invention relates to an input/output bus cycle control circuit, and in further detail, an input/output bus cycle control circuit

[1]Number in the margin indicates pagination in the foreign text.

capable of inserting an idle clock within the input/output bus cycle according to an input/output command in a system controlled by a microprocessor.

Prior Art

In general, when a microprocessor accesses a peripheral device according to an input/output command, it requires a certain recovery time between an input/output bus cycle and the following input/output bus cycle thereof and does not perform access to the same peripheral device in this period. Thus, a conventional microprocessor was equipped with a register that can be set directly with a clock. When one input/output bus cycle ended, this microprocessor inserted the number of idle clocks set by this register, and suspended the start of the following input/output bus cycle in that case to ensure the recovery time between these input/output bus cycles. /370

Problems to be Solved by the Invention

With the above-mentioned conventional microprocessor, the recovery time is set according to the value of the number of clocks. Therefore, the recovery time thus set changes depending on the frequency at which the system thereof operates. For example, if the system operated at a certain frequency is set with the appropriate recovery time, with respect to a system which operates based on a higher frequency, the recovery time is too short, and conversely, the recovery time is unnecessarily long for a system having a low frequency. Therefore, it was necessary to reset the recovery time in association with the frequency at which the system operated, and the program used for setting the recovery time had to be corrected each time.

In addition, if the recovery time was set in association with the maximum frequency thus anticipated to avoid resetting of the recovery time, when this microprocessor is used in a system operated on the basis of a low frequency, a considerable reduction in the performance may be incurred by the system in use.

Therefore, an object of the present invention is to provide an input/output bus cycle control circuit, which solved the above-mentioned problems of the prior art and in which the recovery time does not vary even if the operating frequency of the system changes.

Means for Solving the Problems

In accordance with the present invention is provided a circuit in which an idle clock is inserted between the end of an input/output bus cycle and the start of the following input/output bus cycle of a system controlled by a microprocessor; with an input/output bus cycle control circuit characterized by being equipped with a 1st storage means for storing the recovery time of a peripheral device, a detecting means terminal for detecting the operating frequency of the aforesaid system, a converting means for converting the recovery time stored in the aforesaid 1st storage means to the number of idle clocks associated with the operating frequency of the aforesaid system, and a 2nd storage means for storing the number of idle clocks found by the aforesaid converting means; and always inserting the correct idle clock within the input/output bus cycle even if the operating frequency of the system changes.

Effects

The input/output bus cycle control circuit of the present invention stores the recovery time of a peripheral device and sets the number of idle clocks in association with the systems operating clock. Consequently, even if the system operating clock changes, the correct recovery time always can be set on target within the input/output bus cycle.

Although the present invention will now be described in further detail through the practical examples, the following disclosures are merely practical examples of the present invention are not intended to restrict the technical scope of the present invention.

Practical Examples

A block diagram of the 1st practical example of the input/output bus cycle control circuit of the practical example is shown in Figure 1.

In the input/output bus cycle control circuit in Figure 1, a converter 103 uses the recovery time of a peripheral device as the contents of a recovery time setup register 101 stored in units of ns (nanoseconds) and the signal states of frequency selection terminals 118, 119, 120 and 121 as inputs to change the recovery time to the number of clocks. A switch 122 connects a power supply line 123 or a ground (GND) line 124 to these frequency selection terminals 118 to 121 according to the system operating frequency, whereby a signal "1" or "0" is applied. The output of the converter 103 is outputted to and stored in a recovery clock quantity designation register 105. The data stored in this recovery clock quantity designation register 105, is inputted into a counter 107 by way of a data bus 106, and this counter 107 performs a countdown in accordance with a clock signal

111. A bus cycle control section 109 receives the request signals 113 and 114 and ready signal 110 outputted by a bus cycle request section 108 that accepts input/output requests from peripheral equipment, the zero detection signal 112 of the counter 107 and outputs a control signal to each section.

The operation of the input/output bus cycle control circuit of the present invention above will now be described. An operation in which the number of recovery clocks stored in the recovery clock quantity designation register 105 is inserted in a continuous input/output bus cycle will be described first. If the bus cycle request section 108 receives /371 a request for input/output from peripheral equipment, it sets the request signal 114 to "1" and notifies the bus cycle control section 109 of this, which bus cycle control section 109 sets the input/output bus signal start signal 117 to "1" and actuates the input/output bus cycle. This input/output bus cycle ends when the ready signal 110 becomes "1" and the input/output bus cycle end signal 115 becomes "1" at the same time. The counter 107 loads the contents of the recovery clock quantity designation register 105 by way of the data bus 106 when the input/output bus cycle end signal 115 becomes "1," and performs a countdown in accordance with the clock signal 111. When the counter 107 performs a counting operation, the zero detection signal 112 of the counter 107 becomes "0." When this zero detection signal 112 becomes "0," the bus cycle control section 109 does not accept the input/output bus cycle request signal 114.

When the counter 107 ends the countdown, the zero detection signal 112 becomes "1," the bus cycle control section 109 accepts the input/output

bus cycle request signal 114 and permits actuation of the input/output bus cycle. The memory bus cycle request signal 113 is accepted by the bus cycle control section 109 regardless of the value of the zero detection signal line 112.

The input/output bus cycle control circuit of this practical example, as described above, inserts a number of idle clocks designated by the recovery clock quantity designation register 105 during two input/output bus cycles without fail even if the input/output bus cycle is continuous.

A procedure for setting the number of idle clocks in the input/output bus cycle control circuit of the present invention above is described next.

The frequency selection terminals 118, 119, 120 and 121 are set with, e.g., the switch 122, as described below, in association with the system operating frequency. This switch 122 is so set that if the operating frequency is 3 MHz or less, "1" is applied to the terminal 118 and "0" is applied to the terminals 119 to 121. If the operating frequency is greater than 3 MHz to at most 7 MHz, "1" is applied to the terminal 119, while "0" is applied to the remaining terminals 118, 120 and 121. And if the operating frequency is greater than 7 MHz to at most 15 MHz, "1" is applied to the terminal 120, while "0" is applied to the remaining terminals 118, 119 and 121. If the operating frequency is greater than 15 MHz to at most 30 MHz, a "1" is applied to the terminal 121, and "0" is applied to the remaining terminals 118, 119 and 120.

The converter 103 fetches the contents of the recovery time setup register 101 by way of a data bus 102, performs conversion in accordance

with the signal values of terminals 118, 119, 120 and 121, and that value is stored in the recovery clock quantity designation register 105 by way of a data bus 104.

Here, a detailed operation of the converter 103 will be described with reference to Figure 2. In Figure 2 is shown a block diagram of the converter 103. The converter 103 in Figure 2 is equipped with a shifter 201 which shifts the value of the data bus 102 5 bits to the right, a shifter 202 which shifts the output of the shifter 201 1 bit to the right, a shifter 203 which shifts the output of the shifter 202 1 bit to the right, and a shifter 204 which shifts the output of the shifter 203 1 bit to the right. Furthermore, the outputs of the shifters 201 to 204 are open when the respective frequency selection terminals 118, 119, 120 and 121 are "1" and connected respectively to the data bus 104 via transfer gates 205, 206, 207 and 208 closed when they are "0."

For example, the recovery time setup register 101 is set to 400 ns ("110010000" in a binary), and the operating frequency is 6 MHz. In this case, the terminal 119 is set to "1" while the remaining terminals 118, 120 and 121 are set to "0." Only the transfer gate 207 is open. As a consequence, the output of the shifter 203 is inputted into the recovery clock quantity designation register 105 via the data bus 104. The shifter 203 outputs a 3 ("11" in binary) and is stored in the recovery clock quantity designation register 105. In this case, the actual recovery time is 500 ns (=1 sec/6 MHz×3).

Here, the operating frequency is changed to 14 MHz. In this case, the terminal 120 is set to "1," while the remaining terminals 118, 119

and 121 are set to "0." Only the transfer gate 206 is open. Therefore, the output "6" ("110" in binary) of the shifter 202 is inputted /372 into the recovery clock quantity designation register 105. In this case, the actual recovery time is 428 ns (=1 ns/14 MHz×6).

As described above, even if the system operating frequency varies, the recovery time can be maintained at an appropriate value at or greater than the set value. In addition, in the input/output bus cycle control circuit of the present invention, the above-mentioned operation is performed automatically if the switch 122 is connected to a switch which changes the system operating frequency.

Practical Example 2

When the frequency changed in Practical Example 1, the application of signals to the frequency selection terminals had to be changed by operating the switch 122. With the input/output bus cycle control circuit of this present invention, signals are applied automatically to the frequency selection terminals 118, 119, 120 and 121.

In Figure 3 is shown a block diagram of the 2nd practical example of the input/output bus cycle control circuit of the present invention. The input/output bus cycle control circuit of this practical example is equipped with a frequency measuring instrument 302 and a comparator 303 in place of the switch 122 in Practical Example 1. The remaining configuration is entirely the same as that of the circuit of Practical Example 1; hence, a description will be centered around the parts that are different than in Practical Example 1.

With the input/output bus cycle control circuit of this practical

example, the frequency selection terminals 118, 119, 120 and 121 are connected to the comparator 303. The frequency measuring instrument 302 inputs a clock signal 301 to measure the system operating frequency and output it to the comparator 303. This comparator 303 discriminates the frequency value inputted from the frequency measuring instrument 302, and if the frequency is at or less than 3 MHz, the terminal 118 is set to "1," while the remaining terminals 119, 120 and 121 are set to "0." Hereinafter, in wholly the same way as the setup of the switch 122 of Practical Example 1, the terminal 119 is set to "1" if the frequency value is from 3 to 7 MHz, while the remaining terminals 119, 120, 121 are set to "0." The 120 is set to "1" if the frequency is 7 to 15 MHz, while the remaining terminals 118, 119 and 121 are set to "0." Moreover, when the frequency is 15 to 30 MHz, the terminal 121 is set to "1," while the remaining terminals 118, 119 and 120 are set to "0." The rest of the operation is entirely the same as that of the circuit of Practical Example 1 so a description will be omitted.

As described above, with the input/output bus cycle control circuit of this practical example, the applied values of the terminals 118, 119, 120 and 121 are set automatically even if the frequency is altered, while the value of the recovery time setup register 101 thus set is always updated to the appropriate clock frequency.

Advantages of the Invention

As described above, the input/output bus cycle control circuit of the present invention has a function for being able to convert the recovery time thus set to the number of idle clocks required at any given frequency.

Consequently, correspondence to the change in the system operating frequency is possible with ease, and is most suitable for a system used by switching a plurality of operating frequencies, etc.

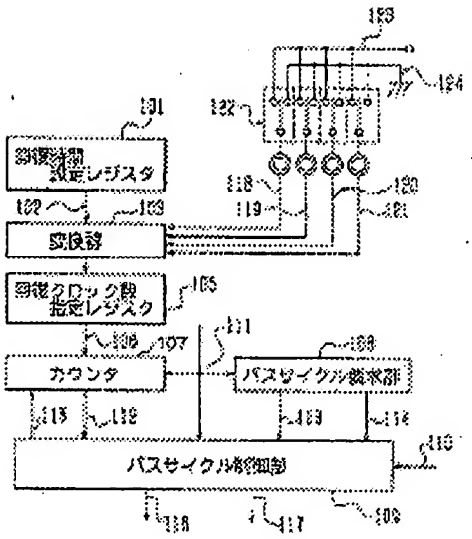
4. Brief Description of the Drawings

Figure 1 is a block diagram of the 1st practical example of the present invention; Figure 2 is a block diagram of the converter 103 in Figure 1; and Figure 3 is a block diagram of the 2nd practical example of the present invention.

(Main Reference Symbols)

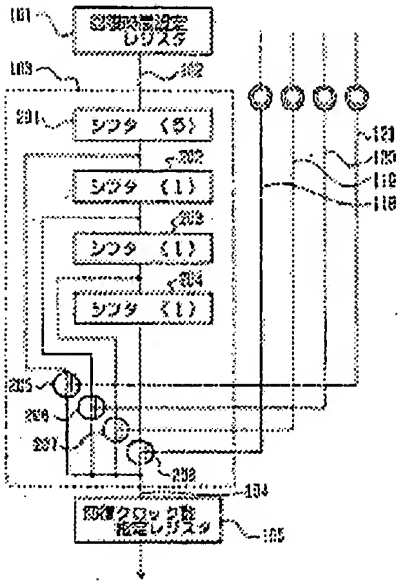
101: recovery time setup register; 102: data bus; 103: converter; 104: data bus; 105: recovery clock quantity designation register; 106: data bus; 107: counter; 108: bus cycle request section; 109: bus cycle control section; 110: ready signal; 111: clock signal; 112: zero detection signal; 113: memory bus cycle request signal; 114: input/output bus cycle request signal; 115: input/output bus cycle end signal; 116: memory /373 bus cycle end signal; 117: input/output bus cycle end signal; 118, 119, 120, 121: frequency selection terminals; 122: switch; 123: power supply line; 124: ground line; 201: shifter of 5 bits to the right; 202, 203, 204: shifters of 1 bit to the right; 205, 206, 207, 208: transfer gates; 301: clock signal; 302: frequency measuring instrument; 303: comparator

Figure 1



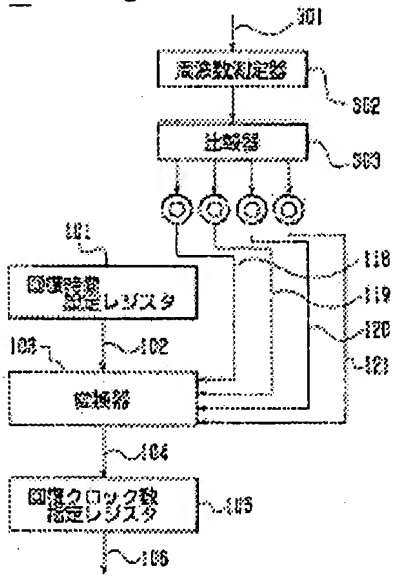
(101) recovery time setup register;
(103) converter;
(105) recovery clock quantity designation register;
(107) counter;
(108) bus cycle request section;
(109) bus cycle control section

Figure 2



(101) recovery time setup register;
(201) shifter (5);
(202) shifter (1);
(203) shifter (1);
(204) shifter (1);
(105) recovery clock quantity designation register

Figure 3



(302) frequency measuring instrument;
(303) comparator;
(101) recovery time setup register;
(103) converter;
(105) recovery clock quantity designation register